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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/991,302	11/13/2001	Balaji Prabhakar	B-3457DIV 619142-7	9884

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EXAMINER	
TRAN, THIEN D	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Supplemental **Office Action Summary**	**Application No.** 09/991,302	**Applicant(s)** PRABHAKAR ET AL.	
	Examiner Thien D. Tran	**Art Unit** 2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20 and 25-32* is/are rejected.

7)☒ Claim(s) *21-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The office action mailed 08/30/2005 is hereby withdrawn.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 5-20, 25-32 are rejected under 35 U.S.C 102(e) as being anticipated by **Cisneros** (U.S Patent No 5,157,654).

-Regarding claims 1, 12, and 15, **Cisneros** discloses a switching system comprising:

a plurality of output 275 stages each operable to supply packets of data to a respective output line (Fig.5, Col.19 line 59 to line 60).

a plurality of input 245 stages each operable to receive packets of data on a respective input line, each received packet being destined for at least a respective one of the output stages (Fig.5, Col.18 line 65).

a transfer stage operable to transfer packets of data from any of the input stages to those of the output stages for which those packets are destined (Col.7 line 35 to line 42, Col.18 line 59 to Col.19 line 53).

each output port connected to an input queuing buffer. In queuing buffer, packets flow in sequence of First in first out order (temporal order, Fig.5 Col.7 line 43 to line 45).

controlling the transfer stage for each output stage, so that the packets destined for that output stage are transferred from the input stage to that output stage in queuing order or noted order (Col.7 line 37 to line 43, Col.19 line 60 to line 25).

-Regarding claim 2, **Cisneros** discloses a switching system comprising:

no more than one packet is received by each input stage during each cell period or time slot (Col.11 line 29 to line 30, line 52 to line 58).

no more than one packet is received by each output stage during each cell period or time slot (Col.11 line 29 to line 30, line 52 to line 58).

no more than one packet is transferred from each input stage by the transfer stage during each stage or phase communication (Col.11 line 52 to line 62).

no more than one packet is transferred to each output stage by the transfer stage during each stage or phase communication (Col.11 line 52 to line 62).

-Regarding claims 5, 6, 7, 8, and 9, **Cisneros** discloses a switching method comprising the following steps occurring during each phase and at each output stage:

selecting the input stage, having that one of the packets which are destined for the output stage which is in first in first out queuing order or earliest in the noted temporal order (Col.7 line 43 to Col.8 line 10).

transferring that one packet from the selected input stage to that output stage unless there is input contention due to the selected input stage also having been selected for another of the output stage (Col.8 line 34 to line 49).

In the case of input contention, selecting the output stage whose destined packet is earliest in the queuing order (Col.8 line 34 to line 49) as recited in claim 6. And repeating the selecting step for each output stage that has not been selected in respect of the next earliest packet in the queuing order as recited in claim 7 (Col.8 line 34 to line 49). If none of the packets is earliest as aforesaid in those output stages, selecting the output stage that has priority information or predetermined ranking (Col.8 line 20) as recited in claim 8. And repeating the selecting step again as recited in claim 9.

Regarding claims 10, 25 Cisneros disclose that each input stage comprises a plurality of input buffers, one for each output stage, the method further including the step of placing each received packet in that one of the input buffers for the input line on which that packet is received and for the output stage for which that packet is destine (figure 5)

-Regarding claims 11, 13, 14, 26, 28, 29, 31, 32 **Cisneros** discloses a switching system comprising:

a plurality of input buffers, one for each output stage, the method further including the step of placing each received packet in that one of the input buffer for the input line on which that packet is received and for the output stage for which that packet is destined (Fig.5, Col.18 line 55 to Col.19 line 60).

a respective output buffer for the packets, and the packets are output from the respective output buffer to the respective output line in dependence upon the queuing order of the packets in the respective output buffer (Fig.5, Col.18 line 55 to Col.19 line 60).

-Regarding claim 16, **Cisneros** discloses the noting the temporal order comprises adding an priority value (urgency indicator, col.7 lines 28-30) to the packets arriving at any of the input stages.

-Regarding claim 17, **Cisneros** discloses operation of the switching system further comprises the step of placing each packet in each output stage in a position dependent upon the urgency indicator added to the packet (figure 1).

-Regarding claim 18, **Cisneros** discloses for adding an urgency indicator to based on said temporal order, further comprising a said each received packet (col.35 lines 10-20)

-Regarding claim 19, **Cisneros** discloses placing each packet in each output stage in a position dependent upon the urgency indicator added to each received packet (col.34 lines 1-15).

-Regarding claims 20, 27, 30 **Cisneros** discloses a switching system comprising:

a plurality of output 275 stages each operable to supply packets of data to a respective output line (Fig.5, Col.19 line 59 to line 60).

a plurality of input 245 stages each operable to receive packets of data on a respective input line, each received packet being destined for at least a respective one of the output stages (Fig.5, Col.18 line 65).

a transfer stage operable to transfer packets of data from any of the input stages to those of the output stages for which those packets are destined (Col.7 line 35 to line 42, Col.18 line 59 to Col.19 line 53).

each output port connected to an input queuing buffer. In queuing buffer, packets flow in sequence of First in first out order (temporal order, Fig.5 Col.7 line 43 to line 45).

controlling the transfer stage for each output stage, so that the packets destined for that output stage are transferred from the input stage to that output stage in queuing order or noted order (Col.7 line 37 to line 43, Col.19 line 60 to line 25).

the method of operation of the switching system comprising the steps for each output stage, adding a priority ((urgency indicator, col.7 lines 28-30) to each received packet noting the temporal order in which the packets destined for that output stage are received by the input stages; and

controlling the transfer stage so that, for each output stage, the packets destined for that output stage are transferred from the input stage to that output stage based on priority (figure 1).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Cisneros** (U.S Patent No 5,157,654).

Regarding claim 3 and 4, **Cisneros** discloses that each time slot is divided into multiple phases depending on the speed and the number of input lines (Col.4 line 15 to line 21, Col.8 line 10 to line 25).

Cisneros does not specifically disclose that each time slot is divided into two and four phases. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to divide a time slot into two, four or any number of phase in **Cisneros's** system in order to achieve a desired switching rate for the switch to prevent packets blocking at multiple input lines.

Allowable Subject Matter

5. Claims 21-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Thien Tran whose telephone number is (571) 272-3156. The examiner can normally be reached on Monday-Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu, can be reached on (571) 272-3155. Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-2600.

7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have any questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197.

Patent Examiner

Thien Tran

DUC HO
PRIMARY EXAMINER

10-17-05